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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,198	GAUTHIER ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 of the application have been examined.

Information Disclosure Statement

2. Acknowledgment is made of the information disclosure statements filed on March 28, 2001 and August 26, 2003 together with copies of the patents and papers. The patents and papers have been considered in reviewing the claims.

Drawings

3. The drawings submitted on 28 March 2001 are accepted.

Specification

4. The disclosure is objected to because of the following informalities:

In Page 2, Para 0006, "Another prior art method includes connecting on on-chip capacitor between the internal supply leads" appears to be incorrect and it appears that it should be "Another prior art method includes connecting one on-chip capacitor between the internal supply leads".

In Page 3, Para 0009, "Figure 5a shows a schematic 44 of an implementation of the method of Figure 3" appears to be incorrect and it appears that it should be "Figure 5a shows a schematic 44 of an implementation of the method of Figure 4".

In Page 4, Para 0011, "a discharging phase when $V_{inst} < V_{ave}$; and a charging phase when $V_{inst} < V_{ave}$." appears to be incorrect and it appears that it should be, "a discharging phase when $V_{inst} < V_{ave}$; and a charging phase when $V_{inst} > V_{ave}$".

In Page 7, Para 0032, "each of the bump and grid components is then connect by a via 78a-78i" appears to be incorrect and it appears that it should be, "each of the bump and grid components is then connected by a via 78a-78i".

In Page 8, Para 0032, "the nine sections are arranged in a three-by-three grid with the ten channels serving as connections between each of the sections" appears to be incorrect and it appears that it should be, "the nine sections are arranged in a three-by-three grid with the twelve channels serving as connections between each of the sections".

In Page 8, Para 0033, "and ten routing channels 82a-82l" appears to be incorrect and it appears that it should be, "and twelve routing channels 82a-82l".

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1, 2, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Ogawa et al.** (U.S. Patent Application 2002/0011885) and **Herrell et al.** ("Modeling of power distribution systems for high-performance microprocessors", IEEE 1999).

7.1 **Larsson** teaches Resonance and damping in CMOS circuits with on-chip decoupling capacitance. Specifically, as per claim 1, **Larsson** teaches an apparatus for modeling a resonance circuit of a microprocessor (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para

1). **Larsson** does not expressly teach an apparatus for modeling an anti-resonance circuit of a microprocessor. **Evans** teaches an anti-resonance mixing filter implemented using analog components (CL1, L47-51; Fig 1, Fig 2 and Fig 3; CL2, L8-16; CL2, L65 to CL3, L10; CL3, L16-30), as the anti-resonance circuit isolates the oscillations that are amplified when operating at resonant frequencies (CL1, L47-49). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** including an apparatus for modeling a resonance circuit of a microprocessor with the apparatus of **Evans** that included an anti-resonance mixing filter circuit. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and the anti-resonance circuit would isolate the oscillations that would be amplified when operating at resonant frequencies.

Larsson does not expressly teach an apparatus for modeling an anti-resonance circuit of a microprocessor. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

Larsson teaches a load model that simulates the resonance circuit (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach a load model that simulates the anti-resonance circuit. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that included a load model that simulates the resonance circuit with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

Larsson does not expressly teach a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model. **Jackson et al.** teaches a transistor that simulates at least one high frequency capacitor (Fig 1; Page 1, Para 0001, L10-14; Page 1, Para 0007, L1-12; Page 23, Para 0229), as that allows internal circuit configurations of LSI circuit to be accurately simulated with transistor models, interconnected resistance models and capacitance models (Page 1, Para 0007, L7-12); and the transistor description of the LSI model reduces the number of transistors constituting the model (Page 4,

Para 0049, L5-7). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that with the apparatus of **Jackson et al.** that included a transistor that simulated at least one high frequency capacitor. The artisan would have been motivated because that would allow internal circuit configurations of LSI circuit to be accurately simulated with transistor models, interconnected resistance models and capacitance models; and the transistor description of the LSI model would reduce the number of transistors constituting the model.

Larsson does not expressly teach that the transistor is connected in parallel with the load model. **Herrell et al.** teaches that the transistor is connected in parallel with the load model (Page 240, CL1, Para 1, L1-7; Page 240, CL2, Para 2, L1-7; Page 241, CL1, Para 2, L1-3; Page 241, CL2, Para 1, L1-4; Page 241, CL2, Fig 2), as that allows capturing the main features of the power distribution network with a simplified equivalent circuit (Page 241, CL2, Para 1, L1-4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that with the apparatus of **Herrell et al.** that included the transistor connected in parallel with the load model. The artisan would have been motivated because that would allow capturing the main features of the power distribution network with a simplified equivalent circuit.

Larsson teaches a capacitor that simulates an intrinsic capacitance of a section of the microprocessor (Page 850, Fig. 1; Page850, CL1, Para 4; Page 850, CL2, Fig 2). **Larsson** does not expressly teach a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model. **Herrell et al.** teaches that the capacitor is connected in parallel with the load model (Page 240, CL1, Para 1,

L1-7; Page 240, CL2, Para 2, L1-7; Page 241, CL1, Para 2, L1-3; Page 241, CL2, Para 1, L1-4; Page 241, CL2, Fig 2), as that allows capturing the main features of the power distribution network with a simplified equivalent circuit (Page 241, CL2, Para 1, L1-4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that with the apparatus of **Herrell et al.** that included the capacitor connected in parallel with the load model. The artisan would have been motivated because that would allow capturing the main features of the power distribution network with a simplified equivalent circuit.

7.2 As per claim 2, **Larsson, Evans, Jackson et al., Ogawa et al.** and **Herrell et al.** teach the apparatus of claim 1. **Larsson** teaches that the load model simulates the resonance circuit with a resistor (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach that the load model simulates the anti-resonance circuit with a resistor. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that included the load model simulating the resonance circuit with a resistor with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment

consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

7.3 As per Claims 8 and 9, these are rejected based on the same reasoning as Claims 1 and 2, supra. Claims 8 and 9 are method claims reciting the same limitations as Claims 1 and 2, as taught throughout by **Larsson, Evans, Jackson et al., Ogawa et al.** and **Herrell et al.**

8. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Ogawa et al.** (U.S. Patent Application 2002/0011885), **Herrell et al.** ("Modeling of power distribution systems for high-performance microprocessors", IEEE 1999) and **Lane** (U.S. Patent 4,459,566).

8.1 As per claim 3, **Larsson, Evans, Jackson et al., Ogawa et al.** and **Herrell et al.** teach the apparatus of claim 2. **Larsson** does not expressly teach that the resistor is a voltage controlled resistor. **Lane** teaches that the resistor is a voltage controlled resistor (CL1, L65 to CL2, L11), because as per as **Ogawa et al.** the internal impedance of the LSI circuit varies depending on the input signals and voltages at the power terminals and the variations in the internal impedance or resistance makes complicated current waveforms (Page 2, Para 0011, L1-5). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to modify the apparatus of **Larsson** with the apparatus of **Lane** that included the resistor being a voltage controlled resistor. The artisan would have been motivated because the internal impedance of the LSI circuit would vary depending on the input signals and voltages at the power terminals and the variations in the internal impedance or resistance would make complicated current waveforms.

8.2 As per Claim 10, it is rejected based on the same reasoning as Claim 3, supra. Claim 10 is a method claims reciting the same limitations as Claim 3, as taught throughout by **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al. and Lane.**

9. Claims 4-5 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Ogawa et al.** (U.S. Patent Application 2002/0011885), **Herrell et al.** ("Modeling of power distribution systems for high-performance microprocessors", IEEE 1999) and **Culler** (U.S. Patent 6,370,678).

9.1 As per claim 4, **Larsson, Evans, Jackson et al., Ogawa et al.** and **Herrell et al.** teach the apparatus of claim 1. **Larsson** does not expressly teach that the load model simulates the anti-resonance circuit in synchronization with a clock cycle. **Culler** teaches that the load model simulates the anti-resonance circuit in synchronization with a clock cycle (CL3, L30-42; CL4, L49-59), as that allows determining the primary resonant frequencies of the power supply

circuits; the resonant frequency of the on-chip power supply circuit is used as input to the initial floor planning (CL4, L55-59) and to adjust the synthesis of the core logic circuit (Cl5, L24-35). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Culler** that included the load model simulating the anti-resonance circuit in synchronization with a clock cycle. The artisan would have been motivated because that would allow determining the primary resonant frequencies of the power supply circuits; the resonant frequency of the on-chip power supply circuit would be used as input to the initial floor planning and to adjust the synthesis of the core logic circuit.

9.2 As per claim 5, **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al.** and **Culler** teach the apparatus of claim 4. **Larsson** does not expressly teach that the clock cycle is generated by a central processing unit clock. **Culler** teaches that the clock cycle is generated by a central processing unit clock (CL3, L30-31), as the clock cycle affects the resonant frequency of the IC package since many harmonics are present in such clock signals (CL3, L30-35); and it is necessary to determine the resonant frequency of the power circuits so they could be used as inputs to the initial floor planning (Cl4, L55-59). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Culler** that included the clock cycle generated by a central processing unit clock. The artisan would have been motivated because the clock cycle would affect the resonant frequency of the IC package since many harmonics would be present in such clock signals; and it would be necessary to determine the resonant frequency of the power circuits so they could be used as inputs to the initial floor planning.

9.3 As per Claims 11 and 12, these are rejected based on the same reasoning as Claims 4 and 5, supra. Claims 11 and 12 are method claims reciting the same limitations as Claims 4 and 5, as taught throughout by **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al.** and **Culler.**

10. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Ogawa et al.** (U.S. Patent Application 2002/0011885), **Herrell et al.** ("Modeling of power distribution systems for high-performance microprocessors", IEEE 1999), **Culler** (U.S. Patent 6,370,678) and **Kunimoto et al.** (U.S. Patent 5,223,653).

10.1 As per claim 6, **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al.** and **Culler** teach the apparatus of claim 4. **Larsson** does not expressly teach that the load model begins to simulate the anti-resonance circuit on a leading edge of the clock cycle. **Kunimoto et al.** teaches that the load model begins to simulate the anti-resonance circuit on a leading edge of the clock cycle (Fig 1; CL1, L29-37; CL5, L35-37), as the elements of the circuit are selected based on the resonance characteristics of the circuit being simulated (CL1, L29-37). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Kunimoto et al.** that included the load model beginning to simulate the anti-resonance circuit on a leading edge of the clock cycle. The artisan

would have been motivated because the elements of the circuit would be selected based on the resonance characteristics of the circuit being simulated.

10.2 As per Claim 13, it is rejected based on the same reasoning as Claim 6, supra. Claim 13 is a method claims reciting the same limitations as Claim 6, as taught throughout by **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al., Culler** and **Kunimoto et al.**

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Culler** (U.S. Patent 6,370,678).

11.1 As per claim 7, **Larsson** teaches an apparatus for modeling a resonance circuit of a microprocessor (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach an apparatus for modeling an anti-resonance circuit of a microprocessor. **Evans** teaches an anti-resonance mixing filter implemented using analog components (CL1, L47-51; Fig 1, Fig 2 and Fig 3; CL2, L8-16; CL2, L65 to CL3, L10; CL3, L16-30), as the anti-resonance circuit isolates the oscillations that are amplified when operating at resonant frequencies (CL1, L47-49). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** including an apparatus for

modeling a resonance circuit of a microprocessor with the apparatus of **Evans** that included an anti-resonance mixing filter circuit. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and the anti-resonance circuit would isolate the oscillations that would be amplified when operating at resonant frequencies.

Larsson does not expressly teach an apparatus for modeling an anti-resonance circuit of a microprocessor. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

Larsson teaches means for simulating a resonance circuit (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach means for simulating an anti-resonance circuit. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows

determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that included means for simulating a resonance circuit with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow simulating an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

Larsson does not expressly teach means for synchronizing the means for simulating an anti-resonance circuit with a clock signal. **Culler** teaches means for synchronizing the means for simulating an anti-resonance circuit with a clock signal (CL3, L30-42; CL4, L49-59), as that allows determining the primary resonant frequencies of the power supply circuits; the resonant frequency of the on-chip power supply circuit is used as input to the initial floor planning (CL4, L55-59) and to adjust the synthesis of the core logic circuit (Cl5, L24-35). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Culler** that included means for synchronizing the means for simulating an anti-resonance circuit with a clock signal. The artisan would have been motivated because that would allow determining the primary resonant frequencies of the power supply circuits; the resonant frequency of the on-chip power supply circuit would be used as input to the initial floor planning and to adjust the synthesis of the core logic circuit.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
June 25, 2004